REMARKS

Applicants thank the Examiner for the consideration given the present application. Claims 1-24 are pending, of which claims 1, 3, 5, 6, 8, and 10-12 are independent.

Applicants traverse the rejection of claims 1-20 under 35 U.S.C. §103(a) as being unpatentable over Hausauer et al. (U.S. 5,790,870).

With all due respect, the Examiner does not appear to appreciate either the arguments presented in the last response or the fact that Hausauer is concerned with peripheral component interconnect (PCI) buses, not small computer system interface (SCSI) buses.

Hausauer describes a method of handling multiple parity errors that occur on two PCI buses that are bridged together (e.g., note the title and see, e.g., column 1, lines 5-10). The system illustrated in FIG. 1 of Hausauer comprises primary PCI bus 117 and secondary PCI bus 115, which are bridged together by PCI bridge 114. The system also includes an EISA bus that is coupled to the primary PCI bus by PCI-EISA bridge 130 and a SCSI bus (not shown) that is coupled to the secondary PCI bus by SCSI controller 116.

A SCSI controller is a device used to connect one or more SCSI devices to a computer bus. In Hausauer, SCSI controller 116 is connected to PCI bus 115, and SCSI connector 118 is responsible for

transferring data between the SCSI connectors and the PCI bus. The data bus between the SCSI controller and the SCSI devices is known as the "SCSI bus." No SCSI devices are illustrated in FIG. 1 of Hausauer; therefore, the SCSI bus between SCSI controller 116 and the SCSI devices (via SCSI connectors 118) is not illustrated. Hausauer does, however, indicate the SCSI controller is coupled to a plurality of disk drives (column 5, lines 17-28). In addition to EISA bridge 130 and SCSI controller 116, various other PCI devices are coupled to primary and secondary PCI buses 115, 117 by PCI slots 122, 126 (see column 5, lines 29-31 and 38 and 39).

Processor C is coupled to PCI bridge 114 for transferring data to and from the various components (i.e., EISA bridge 130, SCSI controller 116, and devices plugged into PCI slots 112, 126) on two PCI buses 115, 117. During data transfer between the processor and a PCI component, the PCI component can report an error to the processor in the form of a PCI parity error signal. As indicated by Hausauer at column 1, lines 57-65, the PCI parity error signal provides feedback information to the processor to attempt to provide a reliable computer system.

Because there are two PCI buses 115, 117, PCI parity errors that occur on the secondary PCI bus 115 cannot be handled in a manner consistent with PCI parity error signals that occur on primary PCI bus 117 (see column 2, lines, 36-46). Hausauer,

therefore, describes a system in which PCI parity errors occurring on primary and secondary PCI buses 115, 117 are unified before being presented to the processor so that the errors are handled more robustly and consistently (see column 2, lines 46-53). Thus, insofar as the claims of the present application are concerned, Hausauer is concerned with two PCI buses and the handling of PCI parity errors that occur over the two buses.

In rejecting claim 1, the Office Action contends Hausauer discloses a method of operating a SCSI device (i.e., SCSI controller 116) in response to a parity error message received over ***a SCSI bus***. In support of this allegation, the Office Action cites column 7, lines 38-46, and column 8, lines 18-21, of Hausauer. Applicants cannot agree. From the preceding discussion, Hausauer does not describe receiving parity error signals over a ***SCSI bus***. Hausauer is not directed to a SCSI bus, but is concerned only with parity error signals received over a PCI bus. As illustrated in FIG. 3 and as clearly indicated at column 8, line 21, Hausauer's lines 194, 196 are connected to SCSI controller 116 and are part of secondary PCI bus 115. As a result, Hausauer does not describe operating a SCSI device in response to a parity error message received over ***a SCSI bus***.

To expedite prosecution, however, independent claim 1 is amended to indicate the parity error signal is received from a ***SCSI***

initiator device over a SCSI bus. In the Hausauer system, PCI parity error signals are communicated between SCSI controller 116 and system controller 128, which generates and delivers an interrupt to the processor (see column 8, line 48-50 and 66-67). Since neither system controller 128 nor the processor is a SCSI device, Hausauer does not disclose or suggest a method of operating a SCSI device (i.e., SCSI controller 116) in response to a parity error signal received from a ***SCSI initiator device*** over a SCSI bus.

In addition, as discussed on page 12 of the Amendment filed March 14, 2005, the Hausauer system also fails to include the explicit step of ***determining***, in response to a received parity error signal, whether the SCSI controller is in a data transfer state. As noted at column 7, lines 38-46, in response to receiving a parity error signal, SCSI controller 116 either terminates or continues a transaction. However, there is no explicit description of SCSI controller 116 ***determining*** whether the transaction involves a data transfer and then generating a message if the transaction is determined to be a data transfer.

To expedite prosecution, independent claim 1 is amended to require the SCSI-enabled device and the initiator device to be separate devices and for the initiator device to be a SCSI initiator device. Hausauer does not disclose a SCSI controller operable to generate a response message to a SCSI initiator device in response

to a parity error message being received. Similar amendments are made to the remaining independent claims, and the foregoing arguments are equally applicable.

In view of the foregoing amendments and remarks, it is submitted that Hausauer does not render obvious the subject matter of independent claims 1, 3, 5, 6, 8, and 10-12. Claims 2, 4, 7, 9, and 13-20 depend on and are allowable with independent claims. Favorable reconsideration and allowance are deemed in order, and such action is respectfully requested.

To the extent necessary, Applicants hereby request any required extension of time not otherwise requested and hereby authorize the Commissioner to charge any required fees not otherwise provided for, including application processing, extension of time, and extra claims fees, to Deposit Account No. 08-2025.

Respectfully submitted,
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